REMARKS

Claims 17-22 were pending in the case. Claims 23-27 have been added. Claims 23-27 are supported in the specification; see, for example, page 15 line 9 to page 16 line 13, and figures 6A and 6B.

Claims 17-22 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent No. 6,539,541 to Geva ("Geva"). In view of the remarks herein, the rejection is respectfully traversed. Withdrawal and allowance are respectfully requested.

Claim 17

The office action incorrectly alleges that Geva teaches all elements of claim 17.

In the office action's assertion on page 3, paragraph 5 ("Response to Arguments"), the office action appears to be identifying elements such as the processor 102, processor bus 110, etc. of element 100 as "image processing elements." Assuming such an identification to be valid, claim 17 further requires "a circuit that stores first states of said image processing elements at a time of a specified image processing result." There is no teaching or suggestion in Geva that such a circuit exists, or that the state of elements 102-138 be stored at all.

The office action asserts that the states of the iterations of the loop correspond to the states of claim 17. However, the states recited in claim 17 are states of image processing elements. Again assuming that the identification of the elements 102-138 as image processing elements is valid, the early exit circuit would need to determine a completion of a calculation based on comparing current states of elements 102-138 (which would need to be stored in a circuit) with first states.

There is absolutely no such teaching in Geva.

Claim 17 is thus clearly patentable over Geva.

For at least the reasons stated above, as well as the reasons stated in the reply filed 12/11/03, claim 17 is patentable over Geva.

Claims 18-22 depend from claim 17, and are therefore patentable for at least the reasons stated above with respect to claim 17. The claims are further patentable for the reasons stated in the reply filed 12/11/03.

Claims 23-27

Applicant has added claims 23-27 directed to particular implementations of an image processing system. Geva does not teach or suggest the features of claims 23-27.

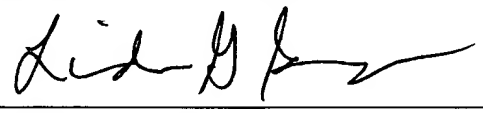
For example, Geva does not teach or suggest "a combinational logic a combinational logic circuit in

communication with the plurality of image processing elements, the combinational logic circuit coded with at least one early exit state defining an early exit condition for the image processing calculation," as recited in claim 23. Geva further does not teach or suggest "a hardware status register in communication with the plurality of image processing elements, the hardware status register loaded with a value representing at least one early exit state defining an early exit condition for the image processing calculation," as recited in claim 26. Geva further does not teach that "the plurality of image processing elements comprises N accumulators, and wherein the at least one early exit state is chosen from N^2 possible states of the N accumulators," as recited in claims 24 and 27. Therefore, new claims 23-27 are clearly patentable over Geva.

Applicant asks that all claims be allowed. Enclosed is a check for $262.00 excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 05/12/04



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